Selecting the Right Power Semiconductors for Multi-MHz Power Converters

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September 1, 2020
Introduction
Multi-MHz Power Converters: Market and Applications

**Wireless Power**
- 6.78 MHz, 13.56 MHz DC-DC systems
- At higher frequency, coils are smaller and cheaper, safety and regulation are improved [Airfuel].
  
  [Source: Nucurrent]

**Plasma Generation**
- 13.56 MHz, 40.68 MHz DC-RF Inverters.
- High Power and Efficient: (100’s of W to 10’s of kW).
- Semiconductor etchers, spacecraft propulsion.
  
  [Source: Liang et al., JESTPE 2017]

**Magnetic Resonance Imaging**
- RF generators for high-frequency magnetic fields.
  
  [Source: Radiology Affiliates Imaging]
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Areas of Investigations

**Control**

![Control Diagram]

Periods become shorter and delays in feedback become more challenging.

**EMI**

![EMI Diagram]

Higher frequency current creates noise that propagates farther.

**Magnetics**

![Magnetics Diagram]

Core loss and winding loss increase with frequency.

**Semiconductors**

![Semiconductors Diagram]

Switching loss increases with frequency.
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Switching loss increases with frequency.
Soft-switching Enables High-Frequency Power Electronics

Hard-Switching

- Switching loss $\propto f_{sw}$.
- Efficiency $\downarrow$ as $f_{sw} \uparrow$. 
Soft-switching Enables High-Frequency Power Electronics

- Switching loss $\propto f_{sw}$.
- Efficiency $\downarrow$ as $f_{sw} \uparrow$.
- Adding additional resonant elements enables soft-switching.
Frequency vs. Conduction Loss Tradeoff

- When $f_{sw} \uparrow$, $L$ and $C \downarrow$.
- This includes the power device’s $C_{oss}$.
Frequency vs. Conduction Loss Tradeoff

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- At higher frequencies, for the same breakdown voltage, only higher $R_{on}$ devices can be used.
- Conduction losses ↑, and efficiency ↓.
WBG Devices to the Rescue

For power semiconductors, $sR_{on}$ ($R_{on}$ for a 1 mm$^2$ area) scales with $V_{BV}$,

\[ R_{on} \propto \frac{1}{A} \]

\[ C_{oss} \propto A \]

The Takeaway: WBG devices allow ↓$C_{oss}$ for the same $R_{on}$ and $V_{BV}$ which ↑efficiencies at higher switching frequencies compared to Si.
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- but also depends on material properties.

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![Diagram of Multi-Resonant Network and Load Network]

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![Multi-Resonant Network](image)

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- **Case Study:** 100 W DC-RF resonant inverter using a 600 V GaN device with a second switch in parallel that is always off.
  - The second switch serves as a parallel capacitor.
  - Expect 94% efficiency in simulation, but only get 89%.
  - And both FETs exhibit losses!

The Issue: Actual Current Device Performance at HF

- Same performance is observed in GaN and SiC Schottky diodes.
- Suspected the extra losses are from charging/discharging of the $C_{oss}$ during off-state.

27.12 MHz, 25 W Rectifier

$C_{oss}$ Loss Characterization: Sawyer-Tower Circuit
In 1929: Sawyer and Tower developed a method to characterize dielectric hysteresis in Rochelle Salt.

ROCHELLE SALT AS A DIELECTRIC

BY C. B. SAWYER AND C. H. TOWER
THE BRUSH LABORATORIES, CLEVELAND

(Received November 6, 1929)

Sawyer and Tower, “Rochelle Salt as a Dielectric”, Phys. Rev. 35, 1929
Methodology: Sawyer-Tower Circuit

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- Obtain a $Q-V$ curve for charging...

![Graphs showing $V_{DS}$ vs. time and $V_{DS}$ vs. $Q_{oss}$]
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- Directly measure the voltage across the DUT.
- Obtain the charge stored in the DUT using a lossless and linear reference capacitor \( C_{ref} \).
- Obtain a \( Q-V \) curve for charging and discharging. Hysteresis equates to Losses (\( E_{diss} \)) per Cycle.
In 2014/16: Fedison used the Sawyer-Tower circuit to characterize Si SJ MOSFETs at 200 kHz.

Results indicate certain devices have significant hysteresis.

Fedison and Harrison, “$C_{oss}$ Hysteresis in Advanced Superjunction MOSFETs”, APEC 2016.
Fedison et al., “$C_{oss}$ related energy loss in power MOSFETs used in zero-voltage-switched applications”, APEC 2014.
Our Findings on GaN

▶ **Recently**: We measured commercial GaN-on-Si HEMTs.

▶ Results can be modeled using Steinmetz fitting similar to magnetic core losses.
  - Increases with $V_{DS}$ and $f_{sw}$
  - $P_{diss} = kf^{1.6}V^\beta$

▶ Losses increase with $dV/dt$, indicating devices perform worse at faster frequencies.

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<table>
<thead>
<tr>
<th>$f_{sw}$</th>
<th>$dV/dt$</th>
<th>$E_{diss}$</th>
<th>$P_{diss}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 MHz</td>
<td>70 V/ns</td>
<td>0.7 µJ</td>
<td>7 W</td>
</tr>
<tr>
<td>30 MHz</td>
<td>150 V/ns</td>
<td>0.9 µJ</td>
<td>27 W</td>
</tr>
<tr>
<td>54 MHz</td>
<td>250 V/ns</td>
<td>1.5 µJ</td>
<td>81 W</td>
</tr>
</tbody>
</table>

Our Findings on SiC

- Same study done on SiC MOSFETs and diodes.
- Results indicate $E_{diss}$ is independent of frequency and $dV/dt$, so $P_{diss} \propto f_{sw}$.
- Losses can scale with $f_{sw}$ slower than GaN!

Device Selection Road Map
Total semiconductor losses in soft-switching conditions can be categorized as:

\[ P_{dev} = P_{cond} + P_{C_{oss}} + P_{gate} \]

\[ \downarrow \]

\[ P_{dev} = R_{on}I_{rms}^2 + k_f^{\alpha}V^\beta + f_{sw}C_{iss}V_{gate}^2 \]
Comparing Si, SiC, and GaN Devices

<table>
<thead>
<tr>
<th>Device Type</th>
<th>$sR_{on}$ Characteristics</th>
<th>$V_{BV}$ Values</th>
<th>$P_{Coss}$ Characteristics</th>
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<tr>
<td><strong>Vertical Si MOSFET</strong></td>
<td>High $sR_{on}$, $5.93 \times 10^{-9} V_{BV}^{2.5}$ [Ω cm$^2$]</td>
<td>$2.5 \times 10^{-9} V_{BV}^{2.5}$ [Ω cm$^2$]</td>
<td>$P_{Coss}$∝$f_{sw}^2$, but can be very low for LV devices.</td>
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<td><strong>Si Superjunction MOSFET</strong></td>
<td>Moderate $sR_{on}$, $0.2d^{\frac{5}{4}} V_{BV}$ [Ω cm$^2$]</td>
<td>$d^{\frac{5}{4}} V_{BV}$ [Ω cm$^2$]</td>
<td>$P_{Coss}$ highly variable and unusable for HF/VHF ($E_{loss} / E_{store} \approx 50%$).</td>
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<td>Low $sR_{on}$, $1.2 \times 10^{-11} V_{BV}^{2.5}$ [Ω cm$^2$]</td>
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<td><strong>GaN-on-Si HEMTs</strong></td>
<td>Lowest $sR_{on}$, $3.6 \times 10^{-12} V_{BV}^{\frac{7}{3}}$ [Ω cm$^2$]</td>
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<td>$P_{gate}$: Low $P_{gate}$, small $C_{iss}$ and $V_{gate} \approx 5$ V.</td>
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Comparing Si, SiC, and GaN Devices

**Vertical Si MOSFET**
- High $sR_{on}$, $5.93 \times 10^{-9} V_{BV}^{2.5} \, [\Omega \text{cm}^2]$
- $P_{C_{oss}} \propto f_{sw}^2$, but can be very low for LV devices.

**Si Superjunction MOSFET**
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**Vertical SiC MOSFET**
- Low $sR_{on}$, $1.2 \times 10^{-11} V_{BV}^{2.5} \, [\Omega \text{cm}^2]$
- $P_{C_{oss}} \propto f_{sw}$.

**GaN-on-Si HEMTs**
- Lowest $sR_{on}$, $3.6 \times 10^{-12} V_{BV}^{\frac{7}{3}} \, [\Omega \text{cm}^2]$
- $P_{C_{oss}} \propto f_{sw}^{1.6}$.
Comparing Si, SiC, and GaN Devices

Vertical Si MOSFET
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Vertical SiC MOSFET
- Low $sR_{on}$, $1.2 \times 10^{-11} V_{BV}^{2.5} [\Omega \text{cm}^2]$
- $P_{Coss} \propto f_{sw}$.
- High $P_{gate}$: Large $C_{iss}$ and $V_{gate} \approx 20$ V.

GaN-on-Si HEMTs
- Lowest $sR_{on}$, $3.6 \times 10^{-12} V_{BV}^{\frac{7}{3}} [\Omega \text{cm}^2]$
- $P_{Coss} \propto f_{sw}^{1.6}$.
- Low $P_{gate}$: small $C_{iss}$ and $V_{gate} \approx 5$ V.

Comparing Si, SiC, and GaN Devices

- **Verdict:** GaN and SiC typically preferable over Si for maximum efficiency.
- However, Si can still be used for $\leq 200$ V applications; HV Si devices have much higher $C_{oss}$ losses and $R_{on}$.
- **Caveats:**
  - Cost of WBG devices can be much higher.
  - Thermal dynamics are not considered for simplicity.
  - GaN HEMTs are not avalanche-rated.
Case Study: GaN vs. SiC

- For a fixed voltage application, consider $P_{total} = P_{cond} + P_{Coss}$
For a fixed voltage application, consider $P_{dev} = P_{cond} + P_{Coss}$.

At low $f_{sw}$, $C_{oss}$ losses are negligible, so GaN is favored.
Case Study: GaN vs. SiC

▶ For a fixed voltage application, consider $P_{dev} = P_{cond} + P_{Coss}$
▶ At higher current and higher-frequency, $P_{cond} \gg P_{Coss}$. 
Case Study: GaN vs. SiC

- For a fixed voltage application, consider $P_{\text{dev}} = P_{\text{cond}} + P_{\text{Coss}}$
- At lower current and higher-frequency, $P_{\text{cond}} \ll P_{\text{Coss}}$. 
For a fixed voltage application, consider $P_{dev} = P_{cond} + P_{Coss}$

Fill in the gaps.
For a fixed voltage application, consider $P_{dev} = P_{cond} + P_{Coss} + P_{gate}$

- $P_{gate}$ is much higher in SiC than GaN.
For a fixed voltage application, consider $P_{dev} = P_{cond} + P_{Coss} + P_{gate}$

We observe this with real devices ($\approx 650$ V, 22 A rating).
SiC Gating Solution: Resonant Gating

- $P_{\text{gate}} = f_{\text{sw}} C_{\text{iss}} V_{\text{gate}}^2$ can be reduced with resonant gate drives.
- Demonstrated a 30 MHz resonant gate drive using a SiC device with $5 \times$ lower gating losses.

Origins of $C_{oss}$ Losses: GaN
GaN D-HEMT Power Devices

- GaN is usually grown on Si substrate for power devices.
- GaN and Si have large thermal and lattice mismatches.
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- GaN and Si have large thermal and lattice mismatches.
- Buffer layers are designed as an insulator to reduce mismatch and suppress vertical leakage.
GaN D-HEMT Power Devices

- **Issue 1**: The substrate is usually lightly Boron-doped, p-type Silicon, which results in high substrate resistance.

- Defects and traps exist in the buffer layers.

- Trapping dynamics have been one of the most critical issues in GaN HEMTs.

- $V_{TH}$ and $R_{ON}$ shift

- Dynamic $R_{DS,ON}$, $C_{OSS}$ losses in soft-switching
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  - $V_{TH}$ and $R_{ON}$ shift
  - Dynamic $R_{DS,ON}$
  - $C_{OSS}$ losses in soft-switching
GaN HEMTs: Separating the $C_{OSS}$ Loss Contributions

To better model the $C_{OSS}$ losses, the loss contribution from different layers are separated.

- Resistive loss from lightly doped substrate ($R_{SUB}$)
- Leakage current path from buffer ($R_{GaN}$)
- Trapping related capacitive hysterestic loss from buffer ($C_{GaN}$)

Zhuang et al., IEEE COMPEL 2019.
$C_{OSS}$ Loss with External Substrate Resistance

The loss measured directly across the device does not change much. With higher $R_{EXT}$ value, the additional loss is higher.

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Zhuang et al., IEEE COMPEL 2019.
Surface and Buffer Traps

Two types of traps dominate in GaN HEMTs:

1. **Buffer traps**
   - originated from carbon doping and fabrication process etc.
   - usually deeper traps with high activation energy

2. **Surface traps**
   - originated from dielectric material, mask design etc.
   - usually shallower traps with low activation energy
Surface and Buffer Traps

- To estimate how trapping affects the measured $C_{oss}$ loss - temperature is varied in Sawyer-Tower setup.
- To better capture the trapping dynamics, a Sentaurus TCAD device simulation of the HEMT stack is built and calibrated.
Temperature-Dependent $C_{OSS}$ Loss - Trap-related loss

Above 100°C, $C_{OSS}$ losses are nearly insensitive to temperature.

To estimate the contribution of each loss mechanism, we assume that at 100°C trap-related losses are eliminated.

Zhuang et al., IEEE COMPEL 2019.
Temperature-Dependent $C_{OSS}$ Loss

Charge stored and discharged in output capacitance at $V_{DS} = 400$ V at 24°C (left) and 100°C (right).

The total charge stored is identical (70 nC) but the losses are $3 \times$ higher at room temperature.
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\[ V_{ds} \text{ [V]} \]

\[ Q_{oss} \text{ [nC]} \]
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Temperature-Dependent $C_{OSS}$ Loss - Trap-related loss

- At room temperature, the measured trap-related losses are around 68\% to 80\% of the total $C_{OSS}$ losses.
- Guacci, 2018: 70\% reduction with buffer redesign

Zhuang et al., IEEE COMPEL 2019.
Guacci et al., IEEE TPEL 2018.
From TCAD: $C_{OSS}$ Losses vs. Trapping levels

- A mixed-mode simulation (Sawyer-Tower circuit + HEMT physical stack) is built in Sentaurus TCAD.
- Traps with a wide range of energy levels are added to the buffer layers, and the simulated $C_{OSS}$ is plotted.
- It is observed that the traps that are mainly responsible for $C_{OSS}$ losses is in the range of 0.5eV from valence band.

Zhuang et al., ECCE 2020.


- $C_{oss}$ losses can be separated into contributions from highly-resistive substrate and trapping related buffer layers.

- Identifying trap energy levels and origins can provide guidelines on buffer and fabrication optimizations.
Origins of $C_{oss}$ Losses: SiC
SiC Device Physics and Structures: Incomplete Ionization

- **Incomplete Ionization**: In WBG devices, dopants require more energy and time to form e\(^-\) and h\(^+\) from an excitation.
- Resistance and capacitance of the device structure are dynamic when excited by high-frequency voltage/currents.
**Termination Region**: In vertical power devices, the edges of the die require support of high electric fields.
SiC Devices $C_{oss}$ Losses: The Culprit

- Through collaboration with ON Semi., we used TCAD to identify the loss origins.
- Simulated a 1200 V ON Semi SiC Power MOSFET with incomplete ionization physics activated and deactivated.

SiC Devices $C_{oss}$ Losses: The Culprit

Observation 1: Incomplete ionization explains $C_{oss}$ loss behavior.

Losses are frequency independent with incomplete ionization.

Observation 2: Majority of the $C_{oss}$ losses occur at the termination.

SiC Devices $C_{oss}$ Losses: The Culprit

- **Observation 3**: Trends and values between experiment and simulation match.
- Indicates proper modeling of the device and physics.

SiC Devices $C_{oss}$ Losses: The Culprit

- Tested custom SiC dies from ON Semi. with different termination sizes and patterns.

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**Observation 4:** Different lengths and structures of the termination create different loss trends.

$C_{oss}$ losses increase with termination length.
SiC Devices $C_{oss}$ Losses: The Culprit

- Tested custom SiC dies from ON Semi. with different termination sizes and patterns.
- **Observation 4:** Different lengths and structures of the termination create different loss trends.
- $C_{oss}$ losses increase with termination length.
- Losses scale differently between guard ring (disconnected JTE) and JTE terminations.
  - JTE is better for higher voltages.
  - Guard ring is better for lower voltages.

SiC Devices: Summary

- $C_{oss}$ losses occur mainly due to resistive charging/discharging path through the termination.
- Behavior is controlled by incomplete ionization physics.
- The size and type of termination structure significantly affect losses.
- Leaves an opportunity for better modeling of SiC devices for HF converters and optimization of termination designs.
Conclusion
Other Works

- **Measurement and Modeling:**
  - *Bosch*: Developed a $dV/dt$ (current-controlled) Sawyer-Tower testing method.
  - *EPFL*: Utilized low-cost, nonlinear resonant method to characterize $C_{oss}$ losses.

- **Loss Origins/Mitigation:**
  - *ETH Zurich/Infineon*: Showed that the design of the buffer region influences $C_{oss}$ losses in GaN devices.

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Nikoo et al., “Measurement of Large-Signal $C_{oss}$ and $C_{oss}$ Losses of Transistors Based on Nonlinear Resonance,” TPEL 2020.
Current Performance Benchmarks at MHz Frequency

De-rating devices and understanding the $C_{OSS}$ losses → better performance.

- **Wireless power transfer - 6.78 MHz, 95% DC-DC efficiency Using 150 V Si**

- **Radio frequency Power Amplifier - 40.68 MHz, 90% efficiency**

Current Performance Benchmarks at MHz Frequency

- **De-rating devices and understanding the $C_{OSS}$ losses → better performance.**

- **Wireless power transfer - 6.78 MHz, 95% DC-DC efficiency Using GaN & SiC with Lowest $C_{OSS}$ losses**


- **Radio frequency Power Amplifier - 40.68 MHz, 90% efficiency**

  - DC-TO-RF EFFICIENCY = 89%
  - POWER = 1500 W
  - FREQUENCY = 40.68 MHz

IEEE PELS: Power Semiconductors @ MHz

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## Conclusion

### Symptom
- The $C_{OSS}$ losses inhibit the performance of soft-switching converters in high-frequency applications.

### Diagnosis
- Sawyer-Tower circuit is used to characterize $C_{OSS}$ losses in GaN and SiC devices.
- GaN and SiC have different trends with voltage and frequency.

### Treatment
- For GaN: Identifying trap energy levels and optimization on buffer design is critical in reducing $C_{OSS}$ losses.
- For SiC: understanding and improving the termination structure is the top priority for better high-frequency performance.
References

Loss Measurements and Characterizations:

Pinpointing Physical Mechanisms:

Modeling the Dynamic Behavior:
## Acknowledgments

### Sponsors
- Stanford SystemX Alliance: ONSemiconductor, Daihen, Texas Instruments, LAM Research
- The Precourt Institute for Energy & the TomKat Center for Sustainable Energy
- National Science Foundation

### Students and Collaborators
- **Superlab**
  - Students: Zikang Tong, Jia Zhuang, Kawin Surakitbovorn, Sanghyeon Park, Weston Braun, Jia Le Xu, Zhechi Ye, Carla Pinzon, Eric Stolt.
  - Postdoc: Dr. Lei Gu, Dr. Jason Poon.
  - Former students: Prof. Jungwon Choi (UMN), Dr. Wei Liang, Dr. Luke Raymond, Dr. Grayson Zulauf.