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An Investigation into the Causes of \( \text{C}_{\text{OSS}} \) Losses in GaN-on-Si HEMTs

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Abstract—In high-frequency, soft-switched power converters, off-state losses from resonantly charging and discharging the semiconductor output capacitor, or “\( \text{C}_{\text{OSS}} \) losses”, have severely limited the achievable performance. In this work, we investigate the origin of these losses in GaN-on-Si High Electron Mobility Transistors (HEMTs) using TCAD simulation and experimental techniques, and find that \( \text{C}_{\text{OSS}} \) losses can be separated into resistive loss and GaN-stack trap related loss. The resistive loss, or \( i^2R \) losses, are a combination of resistance in the GaN stack and the Si substrate, and we detail the effect of displacement current through the highly-resistive substrate layer. The GaN-stack trap-related loss is dominated by trapping dynamics. An estimated contribution percentage from these two dominant loss mechanisms is calculated and presented to focus future efforts on solving these two problems.

Our insights are supported by device simulation and experimental, including supplementing the Sawyer-Tower test technique with external substrate resistors and temperature variation. From device simulation, we observe the expected dependence of substrate displacement current on \( \frac{dV}{dt} \), and the importance of resistive loss is further confirmed with an experimental Sawyer-Tower test with an external resistor attached to the substrate. Under the assumption that the resistive loss is insensitive to temperature change, GaN-stack trap related loss is investigated with the temperature-controlled Sawyer-Tower test, pointing to the criticality of trapping dynamics in \( \text{C}_{\text{OSS}} \) losses.

I. INTRODUCTION

In high-frequency (HF) and very-high-frequency (VHF) power electronics, soft-switched GaN high-electron-mobility-transistors (HEMTs) are widely used to improve power density [1]. In zero-voltage-switched (ZVS) topologies, one version of these soft-switched converters, the voltage across the device is resonantly brought to zero before the device is turned-on, ideally eliminating the dominant switching loss component. This allows the operating frequency to be increased into the MHz range without sacrificing converter efficiency.

At HF/VHF operation, however, recent work has reported new, unexpected losses in these soft-switched GaN HEMTs that occur during the off-state of the switch [2] [3], called “\( \text{C}_{\text{OSS}} \) losses” or “intrinsic energy” in the literature. In high-voltage, high-frequency applications, these additional power losses are on the order of watts, and represent a key barrier to achieving high efficiency and high power density. One recent paper [4] reported an improvement in \( \text{C}_{\text{OSS}} \) losses in GaN HEMTs by altering the buffer layer, but no simulated results were presented.

We implement a customized depletion mode (D-mode) GaN-on-Si HEMT from ON Semiconductor in Sentaurus® TCAD simulations and monitor the displacement current paths during \( \text{C}_{\text{OSS}} \) charge and discharge. Different circuit measurements are reported with customized and commercially-available HEMTs to determine the key loss mechanisms, highlighting potential approaches to mitigating these \( \text{C}_{\text{OSS}} \) losses.

The aim of this paper is to separate and understand the origins of \( \text{C}_{\text{OSS}} \) losses in GaN lateral devices with both TCAD simulation and experimental techniques. More specifically, we find three key loss mechanisms: GaN stack resistive loss, Si-substrate resistive loss, and GaN-stack trap-related loss. The factors and contributions from each loss mechanism – resistive loss and trap-related loss - are studied in-depth in the remainder of the paper.

II. GaN HEMT STRUCTURE

The device simulated in TCAD Sentaurus® is a normally-on AlGaN/GaN structure on a p-type silicon substrate, with its representative schematic shown in Figure 1. In the TCAD, we...
model this complicated as a simplified version of a depletion-mode HEMT, or D-HEMT. While the GaN HEMT structure is familiar, we highlight a couple of key elements to frame the investigation into the key elements of $C_{OSS}$ losses.

Deep acceptors, like Carbon, are usually introduced to the buffer and superlattice stacks between the GaN channel and the Si substrate to suppress off-state leakage current and punch-through induced breakdown [5]. These deep level traps, however, could be strongly impacted by the high electric field that exists when the power device is off in a soft-switched converter (high voltage between the drain node and the source/substrate nodes). In particular, we suspect these deep-level traps could have uneven charging and discharging time constants.

The substrate is typically Boron-doped, p-type Silicon with doping concentration between $10^{14}$ to $10^{15}$ cm$^{-3}$, with the p-type selected because leakage current in p-Si substrates is better sustained by carrier generation during depletion [6]. Depending on the active die area and substrate layer thickness, this can result in a relatively high resistance for the substrate.

We implement this D-HEMT stack in TCAD to investigate and understand the effect of a) the different types and levels of traps in the buffer layers and b) the substrate resistivity on the magnitude of $C_{OSS}$ losses. The simulated substrate thickness is kept constant at 0.03 cm while the doping concentration and die area are varied within a typical range for GaN HEMT manufacturers. The doping concentration for Si is simulated at the typical values of $10^{14}$ cm$^{-3}$, $5 \times 10^{14}$ cm$^{-3}$, $10^{15}$ cm$^{-3}$, and $5 \times 10^{15}$ cm$^{-3}$ [7].

A physical circuit representation of the HEMT in Figure 1 links the stack characteristics with a circuit-equivalent electrical behavior. $R_{GaN}$ models the resistance in the GaN-stack layers, which is primarily caused by the carbon doping in the epitaxial (epi) layer. This carbon doping in the epitaxy is introduced to the GaN-stack to reduce buffer leakage and dynamic $R_{DS,ON}$ [8], but with a higher carbon doping profile, the effective $R_{GaN}$ will be higher, and this is known as one of the dominant causes of $C_{OSS}$ losses [4].

$C_{GaN}$ models the effective capacitance between the drain pad and the substrate. $R_{leak}$ represents the high impedance leakage path for vertical leakage current. We propose that the behavior of the GaN-stack loss can be modeled by the parallel combination of the $R_{GaN}C_{GaN}$ time constant and $R_{leak}$, which is much larger than $R_{GaN}$ and $R_{Si}$ (see Fig. 1). $R_{Si}$ represents the resistance of the substrate layer, and depends only on the thickness, doping concentration and die area. The effect of $R_{Si}$ on $C_{OSS}$ losses will be explained in next section.

III. SUBSTRATE RESISTANCE INDUCED LOSS

A. Substrate Resistance in GaN-on-Si HEMTs

GaN power HEMTs are mostly grown hetero-epitaxially on an Si substrate, since it allows large scale production at lower cost and higher reliability. In commercially-available GaN HEMTs, the Si substrates are p-type doped since the leakage current with p-Si is better sustained (compared to n-Si) by carrier generation in the Si depletion region [6]. The resistance of the Si substrate depends on the doping concentration ($N_A$), the thickness of the substrate layer ($t$) and active device area ($A$) simply as $R_{Si} = \rho_{Si} \frac{t}{A}$. This resistance cannot be optimized on its own, as the substrate composition and thickness affect vertical breakdown voltage, trapping-induced capacitance, current collapse, and power losses in the substrate region itself. High-resistance (lightly-doped) substrates provide better vertical breakdown capability since the depletion region will expand to the substrate layer, which creates additional area that supports the voltage drop, but this larger depletion region also results in higher effective output capacitance and stronger trapping effects [9].

In the TCAD simulation, the substrate thickness is kept constant with 30 $\mu$m and the doping concentration and die area are varied within a typical range used by current manufacturers. The substrate doping concentration is simulated from $10^{14}$ cm$^{-3}$ to $5 \times 10^{15}$ cm$^{-3}$, which is in the range of typical values for commercially available Si wafers [7]. In addition, for modern GaN HEMTs (under 1000 $V_{BE}$), the specific on-resistance is about 3 m$\Omega$·cm$^2$ [10]. We use this to map the simulated device on-resistance (25, 50, 100, and 200 m$\Omega$) to the respective die area (0.12, 0.06, 0.03, 0.015 cm$^2$). Figure 2 plots the substrate resistance against $R_{DS,ON}$, ranging from 25 m$\Omega$ to 200 m$\Omega$, under different substrate doping concentrations $N_A$. Following the simple $R_{Si} = \rho_{Si} \frac{t}{A}$ relationship, $R_{SUB}$ increases with higher $R_{DS,ON}$ and smaller die area. Since die area scales with current rating, devices with higher current rating will have smaller overall substrate resistance.

The effective $R_{SUB}$ varies an order of magnitude (from 0.5 $\Omega$ to over 120 $\Omega$) with the tested change in $N_A$. The high substrate resistance portion of these curves indicate that the substrate resistive loss will likely dominate the $C_{OSS}$ losses for devices with small active die areas.
Across different device manufacturers, the stack design will vary significantly, and particular GaN stacks may implement proprietary technology to suppress the vertical leakage and displacement current through the substrate. We expect, then, that the substrate resistive loss contribution will vary between devices and perhaps even between generations, as GaN HEMT manufacturers fine-tune their processes.

In this section, we see that high substrate currents occur with excitations in the MHz range, and that these currents (and therefore losses) vary with voltage, frequency and waveform shape. Next, we experimentally validate these simulations by conducting a Sawyer-Tower test with an external resistor connected between the substrate source.

C. \( C_{OSS} \) Loss and Varying Substrate Resistance

Without access to device fabrication techniques, it is difficult to alter the substrate doping to directly validate its effect on \( C_{OSS} \) losses. Instead, to approximate the vertical leakage current and the power loss associate with the substrate in commercially-available devices, an external resistor \( R_{EXT} \) is connected between the substrate and source pads of a 650 V device with the substrate terminal not internally connected to the source. By changing the external resistor value, we can estimate the substrate loss percentage and overall trend of vertical leakage currents.

The Sawyer-Tower test (see [2] for detailed operation) is one method to characterize \( C_{OSS} \) losses, and we use this test with the external substrate resistor attached. The general principle of the Sawyer-Tower test is that by connecting a reference capacitor \( C_{REF} \) in series with the non-linear device output capacitance, \( C_{OSS} \), the energy used to charge and discharge \( C_{OSS} \) can be deduced by measuring the voltage across \( C_{REF} \). In this test, the \( C_{OSS} \) losses in the device (DUT) itself are measured both thermally and electrically, and the current through the known \( R_{EXT} \) value is measured directly. We test \( R_{EXT} \) at 1 \( \Omega \) and 5 \( \Omega \) at 1 MHz operating frequency on the aforementioned commercially-available 650 V device.

Figure 4a shows the measured loss directly across the DUT, and as expected, adding the external resistor does not have any measurable influence on the loss in the device itself. The loss across the external resistor – which, as a reminder, approximates increased substrate resistance in a device – is plotted in Figure 4b, and shows a strong dependence on both increasing \( dV/dt \) (increased \( V_{DS} \) results in higher \( dV/dt \) and higher current) and increased substrate resistance. More tangibly, at 300 \( V_{DS} \) and 1 MHz, an extra 0.085 \( \mu \text{J} \) (5 \( \Omega \)) and 0.066 \( \mu \text{J} \) (1 \( \Omega \)) are dissipated in the “substrate” resistances. In a typical device with high substrate resistance, these losses would be in the HEMT itself, causing large \( C_{OSS} \) losses that increase with higher \( dV/dt \).

IV. GaN-stack Related Loss

Depending on the substrate design and vertical displacement current through the substrate, the resistive loss will account for only a portion of total \( C_{OSS} \) losses. Building on prior work [2], [4], we explore the two other major causes of \( C_{OSS} \) losses:

B. Displacement Current through Substrate

Vertical displacement current – the current that flows through the substrate – is a significant portion of the overall off-state current at high electric field and high frequency. Experimentally, it is difficult to extract exact displacement currents with known device characterization techniques, so we use the TCAD simulation to extract different current paths through the HEMT structure. In particular, Figure 3 shows the current through the Si substrate \( (I_{SUB}) \) for a sinusoidal drain-source excitation, where we observe that \( I_{SUB} \) increases substantially with higher drain-source peak voltage \( (V_{DS,max}) \) and with switching frequency.

In this particular simulation, the peak current for a 600 \( V_{DS,max} \), 5 MHz excitation is close to 1 A. With the substrate resistances previously calculated and plotted in Figure 2, which are on the order of \( \Omega \)s or tens of \( \Omega \)s, these currents would indeed result in watts of losses, as measured in [2].

Fig. 3: TCAD simulation shows substrate leakage current is dependent on frequency (top) and \( V_{DS} \) (bottom).
the resistive nature of the C-related defect bands and electron trapping and detrapping dynamics in the GaN stack.

A. Background

The GaN-stack traps refer to the deep trap levels that are located in the buffer layers and the substrate. In general, a deep (far from the valence or conduction band) trap can capture mobile, charged carriers and keep them localized in the neighborhood of trapping center. In most HEMT stack designs, the substrate is thick enough that the substrate traps are not effective, and can be ignored [11]. Deep levels in the buffer, however, have a long trap/de-trap time constant, which makes the electrons trapped in these deep levels unable to follow the high frequency $V_{DS}$ change. Hence, they can largely contribute to the hysteretic behavior in $C_{OSS}$ loss characterization shown in [2].

These trap sites in the GaN stack are primarily due to threading dislocations resulting from the large lattice mismatch between the GaN and Si substrate, a well-known problem. The transition structure, or superlattice GaN, is added expressly to mitigate these effects, but the presence of traps is difficult to eliminate with such a large overall lattice mismatch.

There are multiple sources of electrons that can be injected into this buffer stack. Depending on trap concentration and energy levels, the injected carriers can become trapped and reduce the drain current, increasing dynamic $R_{DS,ON}$ (on-state) or $C_{OSS}$ loss (off-state) effects. In operating power conductors, the most common source is when a large bias is...
Because the trap density, and therefore trap-related loss, are highly dependent on the quality and reliability of the physical growth procedure, the experiments are conducted on two customized D-mode HEMTs from the same family and generation (manufactured by ON Semiconductor). Both HEMTs have a voltage rating of 650 V and a typical $R_{ON}$ of 50 mΩ. The temperature-dependent trap effects are investigated in the Sawyer-Tower test with device temperatures ranging from approximately 15°C to 120°C, within the normal operating temperature of power switching devices.

In these tests, the device case temperature is controlled at 15°C, 24°C, 40°C, 50°C, 100°C and 120°C. To better control the ambient and device temperature, a large block of metal is directly attached to the device under test (DUT) to increase its thermal mass. A hot plate or water chiller are used to elevate or drop the system’s temperature, and the temperatures of the tested device are measured using a FLIR thermal camera.

Figures 5a and 5b plot the $C_{OSS}$ losses for the two devices across this temperature variation at 1 MHz. At 24°C (room-temperature), the measured $C_{OSS}$ losses are similar between the two devices, with a difference of only 0.1 µJ. As the temperature is increased (the DUT case temperature is heated up to the target temperature with variation of $\pm 2^\circ$), a clear and consistent reduction in $C_{OSS}$ loss is observed. For case temperatures above 100°C, the $C_{OSS}$ loss reduction ceases and the remaining losses appear relatively insensitive to temperature. For case temperatures above 100°C, the $C_{OSS}$ loss reduction ceases and the remaining losses appear relatively insensitive to temperature. For device A (fig.5a), the reduction from room-temperature losses is approximately 44% at 50°C and 68% at 100°C (at 400 $V_{DS}$). For device B (fig.5b), this same reduction is approximately 33% at 50°C and 63% at 100°C, perhaps indicating variation in the density or levels of traps between the two devices from the same family. As the temperature is reduced, (down to 10°C for device A and 15°C for device B), the measured $C_{OSS}$ loss again decreases with respect to 24°C data. Taken together, these findings indicate that room temperature is actually the worst-case condition for the $C_{OSS}$ losses in the tested HEMTs.

Figure 6a and 6b summarize the $C_{OSS}$ loss trend with respect to case temperature at 200 to 500 $V_{DS}$. The trend is consistent across drain-source voltage and devices – $C_{OSS}$ losses peak near room-temperature, and decrease significantly at much higher temperatures. We attribute the reduction in $C_{OSS}$ losses at higher temperatures to more energetic carriers in the trapping sites, which can escape more easily and therefore better able to follow the high $dV/dt$ signals applied here. In circuit terms, this can also be explained as a decrease in the detrapping time constant.

To highlight this effect, Figure 7 plots the charge stored and discharged in the output capacitor during the device off-state at $V_{DS} = 400$ V at room temperature and 100°C. The total $C_{OSS}$ loss is calculated as the (integrated) difference between the charging and discharging curves, and can be represented as the hysteresis area between curves. The hysteresis area at room temperature is clearly larger than at 100°C, which results in a larger charge loss and $C_{OSS}$ energy loss. The total charge stored at 400 V in both temperature conditions

![Graph showing $C_{OSS}$ losses vs. case temperature](image)

Fig. 6: $C_{OSS}$ losses for the tested D-HEMTs at 200 $V_{DS}$, 300 $V_{DS}$, 400 $V_{DS}$ and 500 $V_{DS}$ for temperatures ranging from 15°C to 100°C, at 1 MHz.

applied between the drain and source terminals, the electrons accelerate in the conducting channel, and then these hot carriers gain enough kinetic energy to be injected into nearby regions (and penetrate into the buffer layer). The conductive Si substrate can also be a potential electron provider to the buffer stack under certain operation conditions.

B. Temperature-Dependent $C_{OSS}$ Losses

The trapping mechanisms described in the previous section are highly-dependent on temperature, while the doped Si resistance and buffer stack resistance are, to the first order, insensitive to changes in temperature [12]. This provides an opportunity to separate the two loss mechanisms through $C_{OSS}$ loss testing with varying temperature, which is performed experimentally in this section.
Fig. 7: Measured \( Q_{OSS} \) during charge and discharge cycles at 1 MHz and 400 \( V_{DS} \).

is approximately the same; hence, the reduction in \( Q_{OSS} \) and corresponding \( C_{OSS} \) loss is mainly due to a decrease in trapping effect, not a reduction in overall stored energy. We hypothesize that the reduction in hysteresis area indicates a faster detrapping time constant during the voltage rampdown.

With this assumption to the cause of the trapping losses, we can say that in the limit of high temperatures, the trapping effects will become negligible. Indeed, at 100°C and 120°C, the \( C_{OSS} \) loss reduction plateaus to a constant value. To ascertain the relative contribution of each loss mechanism, we assume that the remaining \( C_{OSS} \) losses at 100°C are losses entirely due to the substrate and buffer resistances. With this simplifying assumption, we extract the percent of total losses attributed to the GaN-stack trap loss from 10°C to 50°C, plotted in Figure 8. For both devices, we estimate that trap-related losses contribute between 50 and 70% of the total \( C_{OSS} \) losses, with the deviation across \( V_{ds} \) potentially due to the change in trapping profiles under different bias (electric field) conditions. This assumption and hypothesis is further validated by a comparison with [4], where about 70% of \( C_{OSS} \) losses were eliminated with a buffer stack optimization.

V. CONCLUSION

Reducing \( C_{OSS} \) losses is critical to achieving efficient MHz-frequency power converters. In this paper, we use both TCAD simulation and circuit techniques to determine the driving mechanisms for \( C_{OSS} \) losses. The Si substrate loss
is mainly due to vertical substrate leakage and the highly resistive substrate layer, and is proportional to both $V_{DS,MAX}$ and operating frequency. The GaN-stack loss is dominated by the trapping effect in buffer layers, which is supported by a temperature-controlled Sawyer-Tower characterization. As the device temperature increases, the $C_{OSS}$ loss begins to decrease, which we hypothesize is due to more energetic carriers. However, at higher temperatures, the device exhibits other undesirable characteristics, including higher off-state leakage and higher $R_{DS,ON}$.

The optimization of GaN-on-Si lateral HEMTs for high-frequency applications involves multiple aspects and each electrical parameter must be optimized in combination with the other key drivers. Understanding the relationship between physical stack design and electrical characteristics is essential and valuable. We hope to have provided a roadmap for device designers to consider how to include $C_{OSS}$ loss optimization in at least a subset of their devices that are targeted for high-frequency applications.

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