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Abstract—This paper presents a design methodology for the tuning of a class-D half-wave resonant rectifier with a parallel $LC$ resonant tank input network. Class-D resonant rectifiers offer numerous advantages at high operating frequencies that are leveraged here in the design of a high-voltage rectifier. The absence of a systematic design process, however, has been a limiting factor. Designers have been relying largely on parametric variation during transient simulation to design a rectifier with resistive input impedance at the fundamental frequency of operation. In this paper, we propose a systematic design procedure that begins with universal design curves applicable to any rectifier design of this topology. This is followed by parameter selection and a convergence check that ensures the rectifier operates with the desired output voltage. Experimental results confirm the validity of the design method for both linear and nonlinear resonant capacitances. Based on the outlined procedure, a 25 MHz 500 V rectifier with resistive input impedance is designed and experimentally verified.

I. INTRODUCTION

A class-D resonant rectifier with a parallel $LC$ tank is suitable for high-voltage conversion at high switching frequencies ($>10$ MHz) because of the lower voltage stress on the semiconductor devices and the lower equivalent input impedance at the fundamental of the switching frequency [1]. Moreover, this type of rectifier achieves ZVS transitions across the diodes [2] for high efficiency operation. At high frequencies is also possible to achieve larger voltage gains by connecting in series the output of multiple capacitively isolated rectifiers [3]. Unfortunately, current tuning techniques lack a systematic design approach that accounts for the non-linear behavior of the junction capacitance of the diodes, and/or don't provide a means to find parameters that achieve resistive input impedance [4]–[8]. Consequently, the tuning process has been lengthy, and has not guaranteed the convergence of the output voltage to the intended value under realistic load conditions.

This paper presents a design methodology for a class-D resonant rectifier. The design curve based method allows quick selection of circuit parameters with minimal calculation. The proposed methodology can also predict if the rectifier will converge to the desired output voltage or settle into an unintended operating point. Design curves that are applicable to both linear and nonlinear capacitance are proposed and experimentally verified. A rectifier designed by the proposed methodology is built and tested to show that the circuit behaves as intended.

Section II provides the analysis on the rectifier operation and the theoretical background of the proposed design methodology. Section III illustrates the design procedure by designing a 350 V 27 MHz current-driven rectifier with a resistive input impedance. Section IV presents experimental results to validate the provided circuit analysis and the design example. Section V concludes the paper.

II. ANALYSIS ON THE CLASS-D RECTIFIER

The schematic of the class-D resonant rectifier is shown in Fig. 1a along with its simplified equivalent circuit in Fig. 1b. Notice that the diode’s junction capacitance $C_{j,1}$ and $C_{j,2}$ can be combined with $C_{extra}$ to create an effective resonant capacitance $C$. During operation of the rectifier, the sinusoidal input current $i_s(t)$ resonates with the parallel $LC$ tank of Fig. 1 and clamps the voltage $v_X(t)$ across the diode $D_1$ either to zero or to the output voltage $V_o$. Current flows from ground to the node $X$ when $D_1$ is ON, and from node $X$ to the output.
when $D_2$ is on. Provided that $C_b$ and $C_o$ are large enough to present negligible impedance at the switching frequency, their steady-state behavior can be modelled as a DC voltage source of $V_o/2$ and $V_o$, respectively.

A. Rectifier Input Impedance

Fig. 2 shows the waveforms $v_X(t)$, $i_s(t)$ and $i_o(t)$ of the class D resonant rectifier of Fig. 1a as well as the equivalent circuits during the various commutation intervals within the switching cycle.

![Fig. 2: The rectifier waveforms and equivalent circuits in different operation modes](image)

Here we approximate the fundamental component of $v_X(t)$ waveform in Fig. 2 as a sine wave with $V_o/2$ amplitude and $\theta/2$ phase offset. To justify this approximation, let us look at two extreme cases of the rectifier operating states. At one extreme, the resonant current in the $LC$ tank is large and the capacitor $C$ is charged and discharged very fast. In this case, $v_X(t)$ takes the form of a square wave and the fundamental component of $v_X(t)$ is a sine wave having the amplitude of $\frac{1}{\pi} \cdot (V_o/2) = 1.27(V_o/2)$. At the other extreme where the resonant current is small, the capacitor is charged slowly such that $v_X(t)$ barely reaches $V_o$ (or 0) before it starts to decrease (or increase). Here $v_X(t)$ waveform is close to a triangle wave of which the fundamental component is a sine wave with the amplitude of $\frac{2}{\pi} \cdot (V_o/2) = 0.81(V_o/2)$. The analysis on those two cases reveals that in all the possible operating states between the two extremes the amplitude of the fundamental component of $v_X(t)$ can be approximated to $V_o/2$ with equal to or less than 27% error. Also, in either cases the phase offset of the fundamental component sine wave is roughly $\theta/2$ where $\theta$ represents the phase interval where both $D_1$ and $D_2$ are off. For that reason we approximate the phase offset of the fundamental component of $v_X(t)$ by $\theta/2$.

$Z_{rect}$ is defined as the input impedance of the rectifier at the switching frequency. By the approximation above, the magnitude of the impedance $|Z_{rect}|$ is expressed as

$$|Z_{rect}| \approx \frac{V_o}{2T_s}$$

where $I_s$ is the amplitude of the sinusoidal input current $i_s(t)$. Also, the phase of the impedance $|Z_{rect}|$ can be approximated by

$$|Z_{rect}| \approx \frac{\theta}{2} - \Phi$$

where $\Phi$ is the phase offset of $i_s(t)$.

B. Universal Design Curves

Fig. 3 shows a plot of the analytical solutions of the input-to-output current gain ($I_o/I_s$) (Fig. 3a) and the input impedance phase $|Z_{rect}|$ (Fig. 3b), plotted against $\theta$ and $\omega \sqrt{LC}$.

![Fig. 3: Analytical solution of the class-D resonant rectifier](image)

The solutions are found by imposing the following four conditions on the circuit of Fig. 1b: a) When $D_1$ switches from the ON-state to the OFF-state (at $\phi = 0$ in Fig. 2), the current through $D_1$ is zero, and b) the voltage across the inductor is $-V_o/2$; c) when $D_2$ switches from the OFF-state to the ON-state (at $\phi = \pi$ in Fig. 2), the voltage across the inductor is $V_o/2$; and d) Half a cycle after $D_1$ turns off (at $\phi = \pi$ in Fig. 2), the current through $D_2$ reduces to zero and turns $D_2$ OFF for periodicity.
Fig. 4 shows the analytical solution of \((I_o/I_s)\) and \(|Z_{rect}|\) that are plotted against a new design parameter \(u\) defined as

\[ u := (\omega \sqrt{LC} - 1) \frac{V_o}{I_s \sqrt{L/C}} \]

The definition of \(u\) is constructed such that \((I_o/I_s)\) and \(|Z_{rect}|\) plotted against \(u\) remain almost constant with respect to the vertical axis variable \(\omega \sqrt{LC}\).

![Graph of \(I_o/I_s\) vs. \(u\)](attachment://image1.png)

![Graph of \(|Z_{rect}|\) vs. \(u\)](attachment://image2.png)

Fig. 4: Analytical solution of the rectifier rearranged in terms of parameter \(u\)

Since Fig. 4 plots are roughly independent of \(\omega \sqrt{LC}\), they can be approximated into two-dimensional plots in Fig. 5. The design curves are universally valid for all class-D rectifier designs and are a convenient way of determining various circuit parameters during the rectifier design process.

The curves in Fig. 5 are valid even when the resonant capacitor is nonlinear. The model’s validity with nonlinear capacitance is important because significant portion, if not all, of the resonant capacitor may consist of highly nonlinear diode junction capacitance. To make the model useful for nonlinear capacitance, the effective capacitance \(C_{eff}|V_o\) is introduced. \(C_{eff}|V_o\) is defined as the total amount of charge circulating in the \(LC\) resonant tank divided by the voltage swing \(V_o\), or simply put, the average of the \(C\) vs. \(V\) curve in the range of 0 to \(V_o\). In the class-D rectifier depicted in Fig. 1a, \(C_{eff}|V_o\) is calculated by the following equation:

\[ C_{eff}|V_o = C_{extra} + \frac{2}{I_o} \int \frac{V_o}{V_o} C_j(v)dv \]

where \(C_{extra}\) is parallel-connected linear capacitance and \(C_j(v)\) is the diode junction capacitance at reverse voltage of \(v\) across the diode. \(C_{eff}|V_o\) is used in place of \(C\) when curves in Fig. 5 are used to design a rectifier with nonlinear capacitance.

C. Rectifier Equivalent Circuit

The rectifier in Fig. 1b can be further simplified to the equivalent circuit of Fig. 6.

![Simplified circuit model of the class-D resonant rectifier](attachment://image3.png)

Fig. 6: Simplified circuit model of the class-D resonant rectifier

The curves in Fig. 5 are used to determine the output current \(I_o\), the input reactance \(X_{rect}\) and the input resistance \(R_{rect}\). Once \(u\) is given, the corresponding \(I_o/I_s\) value is obtained from Fig. 5a. \(|Z_{rect}|\) is then obtained by noting that \(|Z_{rect}| \approx \frac{V_o}{2I_s}\) as discussed in Subsection II-A, thus

\[ \frac{I_o}{I_s} = \frac{2I_o}{V_o} \cdot \frac{V_o}{2I_s} \approx \frac{2I_o}{V_o} |Z_{rect}| \]

\(|Z_{rect}|\) for the given \(u\) is also found by simply looking up the corresponding value in Fig. 5b. Finally, \(R_{rect}\) and \(X_{rect}\) are calculated as \(|Z_{rect}| \cos \angle Z_{rect}\) and \(|Z_{rect}| \sin \angle Z_{rect}\), respectively.
$X_{\text{rect}}$ and $R_{\text{rect}}$ may be tailored depending on the design goal. To maximize the overall efficiency, $R_{\text{rect}}$ should be made as large as possible to minimize the influence of the driver’s output resistance. If the design goal is to achieve maximum power transfer, $R_{\text{rect}}$ should be made equal to the driver’s output resistance. In either case, it is desirable to make the input impedance purely resistive or cancel out $jX_{\text{rect}}$ completely by adding an impedance $-jX_{\text{rect}}$ in series.

III. DESIGN OF A CLASS-D CURRENT-DRIVEN RECTIFIER

The design methodology described above is best illustrated by the following example. Consider designing a class-D resonant rectifier of Fig. 1a driven by a sinusoidal current source. We want the circuit to meet the following specifications:

- output voltage $V_o = 350$ V,
- output current $I_o = 70$ mA,
- switching frequency $f = 27$ MHz,
- parallel-connected linear capacitance $C_{\text{extra}} = 107$ pF,
- use two C3D04060E SiC diodes [9] for $D_1$ and $D_2$, with the measured C-V curve in Fig. 7;
- the load at the output $R_L$ is a 5 kΩ resistor;
- the input voltage is in phase with the input current at the switching frequency $f$.

A. First Design

Since the circuit is to be driven by a current source, in order for the voltage and the current to be in phase, $\int Z_{\text{rect}}$ should be zero, which means $u = -0.3$ according to plot in Fig. 5b. Fig. 5a shows $(I_o/I_s)|_{u=-0.3} = 0.3$. Since the required $I_o$ is 70 mA, we set the input current amplitude $I_s$ as $I_s/0.3 = 233$ mA.

The resonant capacitance is the sum of $C_{\text{extra}}$ and two diodes’ junction capacitances $C_{j1}(v)$ and $C_{j2}(v)$, which are highly nonlinear. To calculate $C_{\text{eff}}|_{V_o}$, we integrate $C_j(v)$ of C3D04060E [9] from zero to $V_o = 350$ V, multiply it by two (since $C_{j1}(v)$ and $C_{j2}(v)$ are identical), divide it by $V_o$ and add $C_{\text{extra}}$ to get $C_{\text{eff}}|_{V_o=350}$ V = 166 pF. Combining the obtained $C_{\text{eff}}$ and the definition of $u$, $L$ that makes $u = -0.3$ is found to be 207 nH.

Since the dc-blocking capacitor $C_b$ and the output filter capacitor $C_o$ should exhibit negligible impedance compared to $C_{\text{eff}}$, we choose $C_b = C_o = 50 \cdot C_{\text{eff}} \approx 8$ nF. Table I shows component values of the designed circuit.

B. Convergence Analysis

The next step of the design process is to check the existence of an undesired operating point. If such a point exists, the rectifier driven by a sinusoidal current source might settle into a steady-state operation of undesired $V_o$ and $I_o$. In order to see if the designed circuit has any operating point other than the intended one, graphical analysis is carried out by drawing $I_o$ vs. $V_o$ line and comparing it with the load line for $R_L = 5$ kΩ.

Fig. 8 shows the load line (black dotted line), and the rectifier $I_o$ vs. $V_o$ curve (orange solid line). To draw this curve, $C_{\text{eff}}|_{V_o}$ is evaluated for multiple values of $V_o$ from 0 V to 500 V. This array of $C_{\text{eff}}|_{V_o}$ is entered into the

![Fig. 7: Measured junction capacitance vs. reverse voltage plot of a C3D04060E SiC diode [9].](image_url)

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![Fig. 8: Output current supplied by the 27 MHz rectifier (orange solid line) designed in Subsection III-A, and the current drawn by the 5 kΩ resistive load (black dotted line). Three intersections of two curves are marked by blue dots, from left to right: the undesired convergence point, divergence point, and the desired convergence point. Blue arrows indicate the direction to which the operating point moves.](image_url)
TABLE I: The list of component values for the current-driven rectifier of Fig. 1a designed in Section III

<table>
<thead>
<tr>
<th>$V_o$ [V]</th>
<th>$I_o$ [mA]</th>
<th>$f$ [MHz]</th>
<th>$D_1$, $D_2$ Part Number</th>
<th>$C_{extra}$ [pF]</th>
<th>$R_L$ [kΩ]</th>
<th>$C_o$, $C_b$ [nF]</th>
<th>$L$ [nH]</th>
<th>$I_o$ [mA]</th>
</tr>
</thead>
<tbody>
<tr>
<td>350</td>
<td>70</td>
<td>27</td>
<td>C3D04060E</td>
<td>107</td>
<td>5</td>
<td>8</td>
<td>207</td>
<td>233</td>
</tr>
</tbody>
</table>

C. Redesign

Removing the unwanted convergence point requires change in at least one of the design specifications. Possible remedies include increasing $I_o$, using diodes whose junction capacitance decreases more gradually with voltage, decreasing $V_o$ or $f$. Here we choose to increase $I_o$ from 70 mA to 200 mA and redesign the rectifier. By following the procedure described above, $L$ changes to 202 nH, $R_L$ to 1.75 kΩ, and $I_o$ to 667 mA. The corresponding analysis plot is shown in Fig. 9 by the blue dotted line. The convergence point exists only at $(V_o, I_o) = (350 \text{ V}, 200 \text{ mA})$, meaning that the circuit converges to the desired operating point and the design is complete.

![Rectifier output current - 1.75 kΩ load line](image)

Fig. 9: Output current supplied by the 27 MHz rectifier (orange solid line) redesigned in Subsection III-C, and the current drawn by the new 1.75 kΩ resistive load (black dotted line). The single intersection of two curves, marked by the blue dot, indicates the rectifier always converges to the desired convergence point.

IV. Experimental Results

A. Universal Design Curves

Fig. 10 shows experimental verifications of proposed design curves denoted by dotted lines. Three rectifiers are designed with different resonant inductance, diodes, output voltages and switching frequencies as specified in Table II. Data points are marked on the plots to represent the measured operating state of the rectifiers. The data distribution shows good correlation with the proposed design curves, proving the validity of the presented model.

B. Current-Driven Rectifier Implementation

The 70 W 27 MHz 350 V rectifier designed in Subsection III-C is implemented and shown in Fig. 11. As plotted in Fig. 12, the input voltage and current waveforms are in-phase with phase difference of only 1.6°.

The rectifier represents a resistive input impedance of 251 Ω, which can be adjusted by adding an impedance matching network at the input. The efficiency of the rectifier is 80%. Most of the power loss is due to the large circulating current in the $L^2C$ tank, which can be reduced by choosing a smaller $C_{extra}$ value at the beginning of the design procedure.

V. Conclusion

This paper presented the design methodology of a class-D resonant rectifier. The curve-based design method allows rapid selection of component values and detection of an undesired convergence points. Experiments were conducted to confirm the proposed design curves. A current-driven rectifier based on the proposed methodology was built and tested.

ACKNOWLEDGMENT

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REFERENCES


TABLE II: Rectifier designs for universal design curve verifications in Fig. 10

<table>
<thead>
<tr>
<th>Rectifier No.</th>
<th>$D_1$, $D_2$ Part Number</th>
<th>$C_{extra}$ [pF]</th>
<th>$L$ [nH]</th>
<th>$V_o$ [V]</th>
<th>$f$ [MHz]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>STPSC406B</td>
<td>107</td>
<td>400</td>
<td>200</td>
<td>16.5-28.8</td>
</tr>
<tr>
<td>2</td>
<td>C3D04060E</td>
<td>107</td>
<td>200</td>
<td>350</td>
<td>17.8-33.0</td>
</tr>
<tr>
<td>3</td>
<td>IDD03SG600C</td>
<td>107</td>
<td>600</td>
<td>500</td>
<td>17.0-22.0</td>
</tr>
</tbody>
</table>

TABLE III: Comparison of the rectifier model in Section III and the actual circuit in Fig. 11

<table>
<thead>
<tr>
<th>Model</th>
<th>$I_o$ at $f$ [mA]</th>
<th>$\angle Z_{extra}$ at $f$ [degree]</th>
<th>$V_o$ [V]</th>
<th>$I_o$ [mA]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Experiment</td>
<td>878</td>
<td>1.6°</td>
<td>350</td>
<td>203</td>
</tr>
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</table>

TABLE IV: Comparison of the rectifier model in Section III and the actual circuit in Fig. 11

<table>
<thead>
<tr>
<th>Rectifier No.</th>
<th>$D_1$, $D_2$ Part Number</th>
<th>$C_{extra}$ [pF]</th>
<th>$L$ [nH]</th>
<th>$V_o$ [V]</th>
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<td>107</td>
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<td>17.0-22.0</td>
</tr>
</tbody>
</table>

The authors would like to thank the Energy/Power Management Systems focus area of the SystemX Alliance for funding this work.
Fig. 10: Experimental verification of proposed universal design curves using three different rectifier designs specified in Table II. Proposed model curves are denoted by black dotted lines and corroborating experimental data are marked as colored markers.

Fig. 11: Implementation of the 70 W 27 MHz 350 V current-driven rectifier designed in Subsection III-C

Fig. 12: Measured input current (blue dotted line) and voltage (orange solid line) of the 27 MHz current-driven rectifier at the steady state


